CLAIMS:

What is claimed is:

1. A method of processing a bit transfer operation instruction, comprising:

fetching and decoding a bit value transfer instruction;

executing the bit value transfer instruction on a source bit position of a first data memory location to select a bit value in the source bit position of the first data memory location, the bit position of the first data memory location specified in the bit value transfer instruction;

writing the value to a destination bit position of a second data memory location, the destination bit position specified in the bit value transfer instruction.

2. The method according to claim 1, wherein the step of executing the bit value transfer instruction includes reading an operand at the first memory location.

3. The method according to claim 2, wherein the step of executing the bit value transfer instruction includes copying the bit value at the source bit position of the operand.

4. The method according to claim 3, wherein the step of executing the bit value transfer instruction includes writing the operand to the first memory location.

5. The method according to claim 4, wherein the bit value transfer instruction is a first test bit value transfer instruction.

6. The method according to claim 5, wherein the first test bit value transfer instruction specifies a carry status bit position as the destination bit position of the second memory location.

7. The method according to claim 6, wherein the first test bit value transfer instruction specifies a register as the first data memory location.

8. The method according to claim 6, wherein the first test bit value transfer instruction specifies an address in data memory as the first data memory location.

9. The method according to claim 4, wherein the bit value transfer instruction is a second test bit value transfer instruction.

10. The method according to claim 9, wherein the second test bit value transfer instruction specifies a zero status bit position as the destination bit position of the second memory location.

11. The method according to claim 10, wherein the second test bit value transfer instruction specifies a register as the first data memory location.

12. The method according to claim 10, wherein the second test bit value transfer instruction specifies an address in data memory as the first data memory location.

13. The method according to claim 1, wherein the step of executing the bit value transfer instruction includes reading an operand at the second memory location.

14. The method according to claim 13, wherein the step of executing the bit value transfer instruction includes copying the bit value at the source bit position of the first memory location.

15. The method according to claim 14, wherein the step of executing the bit value transfer instruction includes writing the operand to the second memory location.

16. The method according to claim 15, wherein the bit value transfer instruction is a first write bit value transfer instruction.

17. The method according to claim 16, wherein the first write bit value transfer instruction specifies a zero status bit position as the source bit position of the first memory location.

18. The method according to claim 17, wherein the first write bit value transfer instruction specifies a register as the second data memory location.

19. The method according to claim 17, wherein the first write bit value transfer instruction specifies an address in data memory as the second data memory location.

20. The method according to claim 15, wherein the bit value transfer instruction is a second write bit value transfer instruction.

21. The method according to claim 20, wherein the second write bit value transfer instruction specifies a carry status bit position as the source bit position of the first memory location.

22. The method according to claim 21, wherein the second write bit value transfer instruction specifies a register as the second data memory location.

23. The method according to claim 21, wherein the second write bit value transfer instruction specifies an address in data memory as the second data memory location.

24. A processor for bit transfer operation instruction processing, comprising:

a program memory for storing instructions including a bit value transfer operation instruction;

a program counter for identifying current instructions for processing; and

an arithmetic logic unit (ALU) for executing instructions within the program memory, the ALU including bit value transfer operation logic for executing the bit value transfer operation instruction on a source bit position of a first data memory location to select a bit value in the source bit position of the first data memory location, the bit position of the first data memory location specified in the bit value transfer instruction and writing the value to a destination bit position of a second data memory location, the destination bit position specified in the bit value transfer instruction.

25. The processor according to claim 24, wherein the step of executing the bit value transfer instruction includes the ALU reading an operand at the address in the first memory location.

26. The processor according to claim 25, wherein the step of executing the bit value transfer instruction includes the ALU copying the bit value at the source bit position of the operand.

27. The processor according to claim 26, wherein the step of executing the bit value transfer instruction includes the ALU writing the operand to the address in the first memory location.

28. The processor according to claim 27, wherein the bit value transfer instruction is a first test bit value transfer instruction.

29. The processor according to claim 28, wherein the first test bit value transfer instruction specifies a carry status bit position as the destination bit position of the second memory location.

30. The processor according to claim 29, wherein the first test bit value transfer instruction specifies a register as the first data memory location.

31. The processor according to claim 29, wherein the first test bit value transfer instruction specifies an address in data memory as the first data memory location.

32. The processor according to claim 27, wherein the bit value transfer instruction is a second test bit value transfer instruction.

33. The processor according to claim 32, wherein the second test bit value transfer instruction specifies a zero status bit position as the destination bit position of the second memory location.

34. The processor according to claim 33, wherein the second test bit value transfer instruction specifies a register as the first data memory location.

35. The processor according to claim 33, wherein the second test bit value transfer instruction specifies an address in data memory as the first data memory location.

36. The processor according to claim 24, wherein the step of executing the bit value transfer instruction includes the ALU reading an operand at the address in the second memory location.

37. The processor according to claim 36, wherein the step of executing the bit value transfer instruction includes the ALU copying the bit value at the source bit position of the first memory location.

38. The method according to claim 37, wherein the step of executing the bit value transfer instruction includes the ALU writing the operand to the address in the second memory location.

39. The processor according to claim 38, wherein the bit value transfer instruction is a first write bit value transfer instruction.

40. The processor according to claim 39, wherein the first write bit value transfer instruction specifies a zero status bit position as the source bit position of the first memory location.

41. The processor according to claim 40, wherein the first write bit value transfer instruction specifies a register as the second data memory location.

42. The processor according to claim 40, wherein the first write bit value transfer instruction specifies an address in data memory as the second data memory location.

43. The processor according to claim 38, wherein the bit value transfer instruction is a second write bit value transfer instruction.

44. The processor according to claim 43, wherein the second write bit value transfer instruction specifies a carry status bit position as the source bit position of the first memory location.

45. The processor according to claim 44, wherein the second write bit value transfer instruction specifies a register as the second data memory location.

46. The processor according to claim 44, wherein the second write bit value transfer instruction specifies an address in data memory as the second data memory location.